

REMARKS

Claims 1 and 3-29 are pending in this application. Claims 1, 3, 5, 6, 8, 10, 11, 14-16, 21, 22, and 24-29 are amended. Claim 2 is cancelled. In the Office Action, claims 1-27 are rejected over prior art. Reconsideration of the rejection is respectfully requested.

ELECTION/RESTRICTION

In the present Office Action, the Examiner has indicated that claims 1-27 have been elected for prosecution purposes, and that claims 28-29 are withdrawn from consideration.

Applicants respectfully remind the Examiner that claims 28 and 29 are dependent claims; therefore, these claims are not independent and distinct under 35 U.S.C. 121.

Applicants further respectfully submit in the event of allowance of independent claims 1 and 14, rejoinder of non-elected claims 28-29.

CLAIM REJECTION UNDER 35 U.S.C. §112

Claim 2 is cancelled thereby rendering moot the Examiner's 112 rejection. Claim 3 is amended to remove the Examiner's rejection.

CLAIM OBJECTIONS

Claim 2 is cancelled thereby rendering moot the Examiner's objection. Claim 3 is amended to remove the Examiner's objection.

CLAIM REJECTION UNDER 35 U.S.C. §102

Claims 1-6, 8-10, 12-13, 21-24 and 26 are rejected under 35 U.S.C. § 102(b), as being anticipated by Takizawa (U.S. Patent 6,198,663). The rejection is respectfully traversed.

Takizawa discloses a burn-in test system for only a non-volatile semiconductor memory integrated chip (IC), not a burn-in test program to test multiple kinds of semiconductor devices, e.g., more than one device. See FIGS. 3A-3D, and column 5, lines 47 - column 6, line 29. Takizawa further discloses that the IC integrates a mask ROM 61 having a test routine 61a, i.e., test program. In other words, “the step-by-step processing of the test and judgment of good or bad are carried out by the IC 60 itself as part of the functions of the test routine 61a, the read and write routines as well as the judgment routine are eliminated from the tester 70.” Column 5, lines 23-26.

The present claims recite methods of testing a multi-chip package. Generally, a multi-chip package is a plurality of semiconductor devices stacked together. The semiconductor devices may include a Flash memory, DRAM, and SDRAM. Independent claims 1, 14, 21, and 27 recite that the integrated burn-in test program is adapted to test all the multiple kinds of a semiconductor device. In other words, the test program integrates several different programs capable of testing various types of a semiconductor device, not that the test program itself is integrated into an IC.

Applicants respectfully submit that Takizawa fails to disclose each and every feature of independent claims 1 and 21, it cannot provide a basis for rejection under 35 U.S.C. §102. Accordingly, the Applicants submit that claims 1, 3-6, 8-10, 12-13, 21-24, and 21, are allowable over the prior art. Withdrawal of the rejection is respectfully requested.

CLAIM REJECTION UNDER 35 U.S.C. §103

Claims 14-18, 20 and 27 are rejected under 35 U.S.C. §103(a) as being unpatentable over Takizawa in view of Goins (U.S. Patent 5,931,311,). This rejection is also respectfully traversed.

As discussed above, Takizawa neither discloses nor suggests the claimed invention as recited in independent claims 14 and 27. Claims 14 and 27 also recite in part that the integrated burn-in test program is adapted to test all the different types of a semiconductor device.

For at least these reasons, the Applicants respectfully submit that Takizawa fails to disclose or render obvious individually or in combination the features recited in independent claims 14 and 27, and Goins fails to cure this deficiency. Claims 15-18, and 20, which depend from claim 14 are likewise distinguished over the prior art for at least the reasons discussed as well for the additional features they recite. Reconsideration and withdrawal of the rejection is respectfully requested.

Claims 11 and 25 are rejected under 35 U.S.C. §103(a) as being unpatentable over Takizawa in view of Goins. This rejection is also respectfully traversed.

Claim 11 is dependent to claim 6, which is dependent to independent claim 1. As distinguished over the prior art above against claim 1, claim 11, which further recites additional features, is patentable over the prior art.

Claim 25 is dependent to claim 21. As distinguished over the prior art above against claim 21, claim 25, which further recites additional features, is patentable over the prior art.

Claims 7 and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Takizawa in view of Goins. This rejection is also respectfully traversed.

Claim 7 is dependent to claim 1. As distinguished over the prior art above against claim 1, claim 7, which further recites additional features, is patentable over the prior art.

Claim 19 is dependent to claim 14. As distinguished over the prior art above against claim 14, claim 19, which further recites additional features, is patentable over the prior art.

CONCLUSION

In view of the above remarks, reconsideration of the rejections and allowance of claims 1 and 3-29 are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below. If the Examiner believes that a personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (703) 668-8000.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, PLC

By

John A. Castellano, Reg. No. 35,094

JAC/LYP:jcp

P.O. Box 8910
Reston, VA 20195
(703) 668-8000